# A General Route toward Complete Room Temperature Processing of Printed and High Performance Oxide Electronics

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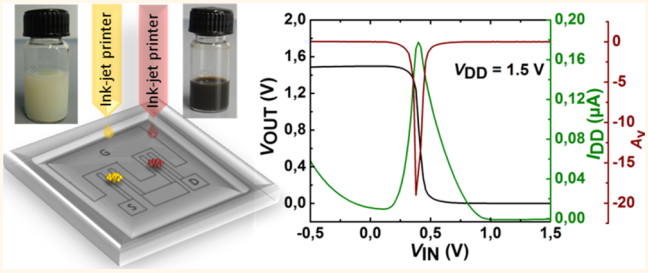
**ABSTRACT** Critical prerequisites for solution-processed/printed field-effect transistors (FETs) and logics are excellent electrical performance including high charge carrier mobility, reliability, high environmental stability and low/preferably room temperature processing. Oxide semiconductors can often fulfill all the above criteria, sometimes even with better promise than their organic counterparts, except for their high process temperature requirement. The need for high annealing/curing temperatures renders oxide FETs rather incompatible to inexpensive, flexible substrates, which are commonly used for high-throughput and roll-to-roll additive manufacturing techniques, such as printing. To overcome this serious limitation, here we demonstrate an alternative approach that enables completely room-temperature processing of printed oxide FETs with device mobility as large as 12.5 $cm^2/(V\ s)$. The key aspect of the present concept is a chemically controlled curing process of the printed nanoparticle ink that provides surprisingly dense thin films and excellent interparticle electrical contacts. In order to demonstrate the versatility of this approach, both *n*-type ($In_2O_3$) and *p*-type ($Cu_2O$) oxide semiconductor nanoparticle dispersions are prepared to fabricate, inkjet printed and completely room temperature processed, all-oxide complementary metal oxide semiconductor (CMOS) invertors that can display significant signal gain (~18) at a supply voltage of only 1.5 V.




**KEYWORDS:** printed electronics · field-effect transistor · oxide electronics · room-temperature processing · chemical curing

Solution processed/printed electronics is a rapidly growing field in material science.[1−3] In accordance with future technological demands, among others, printed logics are presently receiving substantial research attention; the numerous novel application opportunities involving printed logics include radio frequency identification (RFID) tags, intelligent packaging, electronic textiles, electronic papers, disposable medical diagnostics, *etc.*[4−6] Traditionally, solution processed organic semiconductors have been studied for printed, flexible FETs, whereas transistors from inorganic materials (mostly involving inexpensive and nontoxic metal oxides) have been introduced relatively recently. Although oxide semiconductors typically exhibit excellent environmental stability and superior electronic transport properties (such as high intrinsic carrier mobility)[7−9] compared to organics, their successful implementation into printed, high performance devices has remained rather challenging; for example, high performance, solution processed oxide FETs have only been achieved for devices that are fabricated at high temperatures, in particular, above the glass transition temperature of inexpensive, flexible substrates (polymer, cellulose, *etc.*). In fact, the need for high process temperature is on top of the list of challenges that must be overcome for most of the anticipated technological applications. The analysis of literature results shows a direct relationship between the field-effect mobility ($\mu_{FET}$) and the annealing/processing temperatures can be drawn;[10] recent results show high device mobility ($\mu_{FET}$ >100 $cm^2/(V\ s)$)

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for solution-processed oxide FETs that are annealed at higher temperatures[11,12] (at least 400 °C), where $\mu_{FET}$ of less than 1 $cm^2/(V\ s)$ are observed for devices processed at around 150 °C or lower.[10,13,14] Of course, efforts have continuously been made to reduce the process temperatures without compromising on the device performance; to name a few, techniques such as combustion synthesis[15] or sol−gel on chip[16] have been proposed which have resulted in $\mu_{FET}$ values around 10 $cm^2/(V\ s)$ at process temperatures around 200−250 °C. On the other hand, alternative annealing techniques, such as plasma annealing,[17] microwave irradiation[13] and UV curing[18] have also been investigated to replace the thermal annealing step and to keep the substrate temperature low. However, so far, nearly all these techniques require an additional process step and instrumentation which may not be compatible with high-throughput roll-to-roll printing processes. In the given context, here we propose and demonstrate a distinctly different approach to fabricate oxide transistors and logics that allows for complete room temperature processing without an extra process step being involved. The concept includes printing of an oxide semiconductor based nanoparticulate ink to form the transistor channel and a room temperature chemical flocculation process leading to interparticle physical contacts and densification of the printed layer.

In general, nanodispersions can either be stabilized electrostatically with high charge density at the nanoparticle surface or electrosterically which involves grafting or adsorption of stabilizer molecules at the particle surface. In the first case, it is rather not possible to obtain a heavily loaded (particle loading) nanodispersion with sufficient shelf life. As a consequence of the limited particle concentration in such an ink, the printed layers typically become highly porous and inhomogeneous, thereby resulting in limited device performance.[10] On the other hand, with electrosteric stabilization, it is usually possible to have very high nanoparticle loading in the ink along with long shelf life; the adsorbed stabilizer molecules can be very efficient in preventing reagglomeration of particles in the dispersion. However, the established stabilizer molecules are often either insulating or semi-insulating; consequently, they hinder electronic charge transport and hence again an additional heating step at high temperatures is required to remove them. Nevertheless, a solution to this problem can be offered stemming from the studies on relative adhesion stability (or destabilization tendency) of different stabilizer molecules at different pH levels and ionic concentrations. For example, a systematic study involving several polyelectrolytes as polymer stabilizers for magnetic oxide nanoparticles has been reported by Golas *et al.*,[19] where it has been shown that nanoparticles with a polyelectrolyte shell made of poly(sodium acrylate) or poly(sodium vinylphosphate) can be destabilized by addition of an appropriate ionic species, such as NaCl. This phenomenon strongly depends on the pH level and the concentration of the NaCl added to the dispersion. In the following study, it is demonstrated that this approach can also be utilized for low-temperature fabrication of high-performance, printed oxide electronics. By selecting a suitable concentration of an ionic species for the chosen polymer stabilizer and the pH level, the nanoink can be designed in such a manner that on one hand it shows a long shelf life and on the other hand the concentration of the ionic species increases during the ink drying process to quickly reach the critical level. At the critical concentration the stabilizer molecules are removed from the nanoparticle surface leading to interparticle physical contacts and subsequent densification of the nanoparticulate film. A schematic representation of the chemical curing and densification process has been illustrated in Figure 1. In fact, it has been shown for metallic particles that this effect may even induce neck formation and sintering of nanoparticles at room temperature.[20,21] To the best of our knowledge, this technique has never been used for active elements of an electronic device, such as the transistors. As an obvious difference to other low temperature nanoparticle film curing techniques mentioned earlier, this approach does not require any extra process step or additional processing time. Furthermore, the electrical performance is not at all compromised in this process as it can be clearly seen from an unprecedented FET device mobility (12.5 $cm^2/(V\ s)$) of $In_2O_3$ nanoparticle channel *n*-type MOSFET (NMOS). This performance for solution processed oxide FETs is certainly exceptional, in particular when the completely room temperature processing aspect is taken into account. For the fabrication of FETs, a composite solid polymer electrolyte is chosen to serve as the gate insulator, because such polymeric electrolytes (a) show high capacitance and can reduce the drive and gate voltages down to only a few volts and (b) can closely follow the surface topology of the semiconductor films and provide highly conformal semiconductor/dielectric interface even for the rough semiconductor surfaces.[10,11,22]

## RESULTS AND DISCUSSION

**Preparation and Characterization of the Nanoinks.** Sodium salt of poly(acrylic acid) (PAANa) is chosen as the stabilizer; PAANa ligands adsorb to the nanoparticle surface during the ink preparation and thereby reduce the surface energy of the nanoparticles resulting in a reduced tendency for agglomeration. Indeed, the nanoink thus produced is found to be quite stable, at least for the time period of several months (Figure 2a,c). Next, it is found necessary to optimize the concentration of the flocculation agent (in the present study we use NaCl) in such a manner that it does not induce

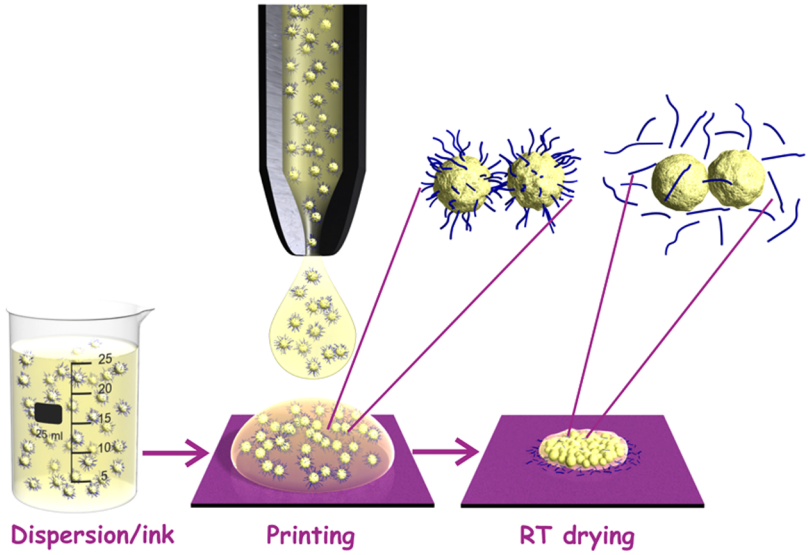


**Figure 1. Schematic representation of the chemically controlled destabilization and flocculation process of the printed nanoink droplets. The NaCl loaded semiconducting oxide nanoinks show spontaneous stabilizer removal from the nanoparticle surface during the ink drying process.**

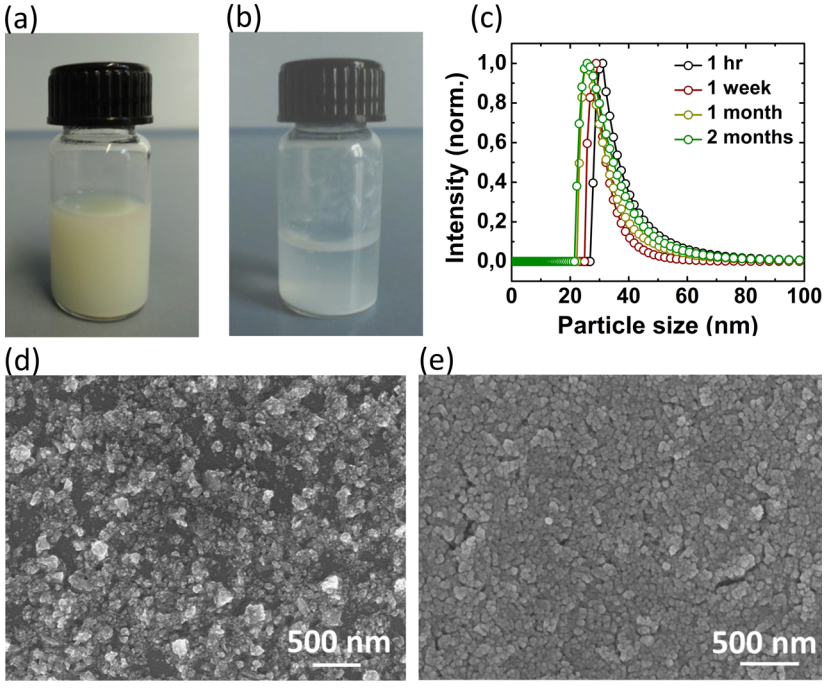


**Figure 2. Stability of the $In_2O_3$ nanoinks with PAANa as the stabilizing ligands and different halide ion concentration. (a) $In_2O_3$ nanoink with 20 mM NaCl, after 2 months of ink preparation; (b) $In_2O_3$ nanoink with 50 mM NaCl, after 1 h of ink preparation; (c) DLS particle size distribution of the $In_2O_3$ nanoink with 20 mM NaCl concentration, as a function of the elapsed time. Surface morphology of the printed $In_2O_3$ thin films, SEM images showing surface topography of the printed droplets from nanoparticulate inks that contain (d) no NaCl and (e) 20 mM NaCl, respectively.**

detachment of the ligands immediately upon addition to the nanodispersion, thereby ensuring sufficiently long shelf life of the inks. However, the concentration of the flocculation agent quickly becomes supercritical during the first phase of the ink drying process so that the ligands are removed from the particle surface, which then allows sufficient time for the nanoparticulate layer densification process to take place. The optimum amount has been found to be 20 mM concentration of NaCl in the formulated nanoink that has shown long-term ink stability. In contrast, a considerably higher concentration (for example, 50 mM NaCl) destabilizes the dispersion rather quickly; nearly all the particles can be found to reagglomerate and settle down already within 1 h of the ink preparation (Figure 2b). On the other hand, the 20 mM NaCl containing nanoink also reaches the critical NaCl concentration during the drying process and desorbs the

PAANa ligands from the $In_2O_3$ particle surface (as has been schematically shown in Figure 1). The strong capillary force acting on the particles during the last phase of the ink drying process establishes interparticle physical contacts and brings all the uncovered particles closer together, resulting in a considerable densification of the nanoparticulate layer, as can be seen from the comparative scanning electron microscope (SEM) images (Figure 2d,e) of the printed $In_2O_3$ layers from the nanoparticulate ink without and with NaCl, respectively. Although it is known that a neutralized poly acrylic acid (PAA) is a conducting polymer (which partially allows interparticle electronic transport even when the nanoparticles are encapsulated by PAANa),[23] the advantage of this chemically controlled stabilizer removal and the nanoparticles densification process is immediately reflected in the $I-V$ measurements performed on the printed layers without and with NaCl additive (see Supporting Information Figure S3). While the electrical transport measurements on the nanoparticle film with intact PAANa shell indicates Schottky contacts and poor conductivity, in contrast, the NaCl treated film shows completely Ohmic behavior and nearly 2 orders of magnitude lower sheet resistance.

Further evidence of the chemical removal of stabilizer molecules due to addition of 20 mM NaCl to the ink is obtained from a systematic and comparative X- ray photoelectron spectroscopy (XPS) study of the chemical structure of thin films with and without NaCl additive in the nanoink. XPS data analysis reveals that the distinct spectral fingerprint of the intact PAANa ligand shells, which is the carboxylic group in the C 1s spectrum, is only present in the printed films prepared from the ink without NaCl, and in contrast is not recognizable for the thin films prepared from NaCl containing nanoink, suggesting the removal of PAANa ligands from the nanoparticle surface. Moreover, the C 1s spectrum of the thin film without NaCl additive changes significantly after several hours of X-ray irradiation and becomes similar to the spectrum of the sample with NaCl additive, whereas the sample with 20 mM NaCl does not have any changes for hours of X-ray irradiation.

**Fabrication and Electrical Characterization of $In_2O_3$ Nanoparticle Channel NMOS Device.** The device fabrication starts with preparation of the passive structures. High quality, surface-polished, soda-lime float glass was used as the substrate; the passive structures are fabricated with sputtered tin doped indium oxide (ITO) and structured using e-beam lithography. All the FETs were prepared with an in-plane FET device geometry.[10,22] After prestructuring of the electrodes, the oxide nanoparticle channel layer was printed using a commercial Dimatix DMP 2831 inkjet printer, followed by printing of a suitably designed composite solid polymer electrolyte on top which served as gate insulator.[22,24−29] The electrolyte dried quickly at room temperature by evaporation of the excess solvent.

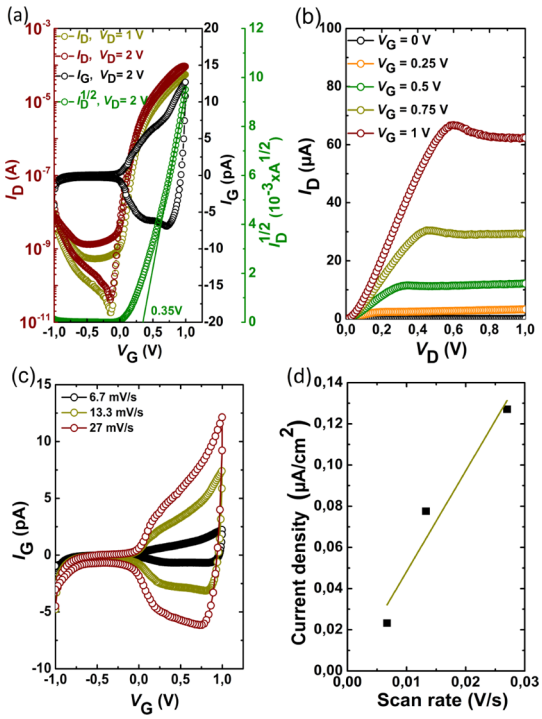


**Figure 3. (a) Transfer characteristics and (b) drain current ($I_D$)−drain voltage ($V_D$) curves of a typical $In_2O_3$ transistor device that is processed completely at room temperature from printed and chemically compacted nanoparticulate films; (c) gate current ($I_G$, displacement current)−gate voltage ($V_G$) relationship of the same FET device showing the voltage scan rate dependence of gate current that is measured with an applied drain voltage ($V_D$) of 2 V; (d) calculated current density (at the saturation regime, at $V_G$ = 1 V) is plotted *versus* the gate voltage scan rates; the slope (4.9 $\mu$F/cm$^2$) provides the specific capacitance ($C_{DL}$) of the semiconducting channel.**

The transistor characteristics were then recorded using an Agilent 4156C parameter analyzer. Figure 3a,b illustrates the transfer and current−voltage curves of a typical $In_2O_3$ channel FET printed from a $In_2O_3$ nanoink containing 20 mM NaCl. The key features (or figures of merit) include high ON/OFF ratio ($I_{ON}/I_{OFF}$) > $10^6$, positive threshold voltage (~0.35 V) (*i.e.*, the FETs operate in accumulation mode), high specific transconductance, $g_m$ of about 3.5 $\mu$S/$\mu$m (transconductance is defined as the drain current dependence on the gate voltage modulations, $g_m = (\partial I_D/\partial V_G)$, and an extremely small subthreshold slope, $S$ (gate voltage modulation required to change the drain current by 1 order of magnitude) of only 78 mV/decade, which is close to the theoretical limit of 60 mV/decade.[30] The other important figure of merit of the FET device, the charge carrier field-effect mobility is calculated from the transconductance in the saturation regime, using the following equation:[31]

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = \text{const.}} = \frac{W\mu_{FET}C(V_G - V_T)}{L} \qquad (1)$$

where, $I_D$ is the drain current, $L$ (~10 $\mu$m) and $W$ (~80 $\mu$m) are the length and width of the printed channel,

respectively; $V_G$ and $V_T$ are the applied gate voltage and the threshold voltage, respectively; and $C$ is the specific capacitance (for electrolyte gated FETs, it is in fact the electrical double layer capacitance, $C_{DL}$). All the other parameters being accurately known, it is necessary to obtain a precise value of $C_{DL}$. Here, the most reliable estimation can be obtained from the displacement/charging current measured on the device itself. In order to ensure precise calculation of $C_{DL}$ of the semiconducting channel, special care is taken to minimize the overlap of the printed electrolyte layer with the passive structures (to avoid displacement current from the ITO electrodes). Next, as shown in Figure 3c, the gate current ($I_G$) is recorded while the gate voltage ($V_G$) is scanned with different scan rates. It can be seen that the displacement/charging current is negligible at the Off-state of the FET, shoots up when the transistor switches on and increases monotonically thereafter for larger positive gate voltages; in fact this feature further confirms the fact that $I_G$ is resulting mostly from the semiconducting channel material, $In_2O_3$, and not from the high conducting ITO (for metallic or metal-like (such as ITO) electrodes, in absence of surface reaction/Faradaic currents, the displacement current should be fairly constant with varying gate voltages).[22] A similar gate voltage dependence of the displacement current in electrolyte-gated FETs has also been observed earlier for organic field-effect transistors.[25,32] It can be noticed here that $I_G$, *i.e.*, the displacement current from the semiconducting channel, increases monotonically with an increasing carrier accumulation at higher positive gate voltages; hence from Figure 3c, it is in fact possible to calculate $C_{DL}$ of the semiconducting $In_2O_3$ channel at any intermediate gate voltage. In order to obtain $C_{DL}$ at the saturation regime, the displacement currents at $V_G = 1$ V are plotted in Figure 3d as a function of $V_G$ scan rates. From this plot $C_{DL}$ is estimated to be 4.9 $\mu$F/cm$^2$ at $V_G = 1$ V (for details see Supporting Information). Substituting this value in eq 1, the calculated $\mu_{FET}$ comes around 12.5 cm$^2$/(V s), which is surprisingly high for completely room temperature processed and printed oxide FETs. In addition, field-effect mobility of the device has also been estimated for different gate voltages in the saturation regime by calculating the instantaneous double layer capacitance and transconductance at every gate potential (Figure S5) and subsequently substituting the values in eq 1. Notably, the calculated mobility values do not vary significantly with varying gate potential.

One may still wonder that a large mobility value of the electrolyte-gated FETs (EG FETs) is of limited importance, as the speed of the EG FETs must be governed by the mobility of ions in the electrolytes. However, this criticism is not fully valid, at least not for the printed FETs. Electrolyte-gating is usually associated with large parasitic currents (due to large capacitance of the electrolytic insulator); when this parasitics are controlled to lower values, the speed of electrolytic polarization can be fast enough for printed electronics, that is the speed of printed FETs are not determined by the electrolytic-polarization time. This is because of the fact that the speed of the printed FETs is strongly limited by the large channel lengths, coming from the low printing resolution of the commercial printers (in the range of tens of micrometers), which is why the polarization time of a high conducting electrolyte systems does not appear to be too high in comparison. In this regard, our earlier publications with oxide semiconductors estimate[22] and demonstrate[29] that electrolyte-gated FETs can attain beyond MHz switching speed; similar results have also been reported by other groups working with either organic semiconductors[26] or carbon nanotubes (CNTs).[33,34]

The performance can further be improved to $\mu_{FET}$ = 14 cm$^2$/(V s) when the printed nanoparticles are annealed at 100 °C, which is still well below the critical temperature of flexible, low-cost substrates. The transfer and current−voltage curves of a typical device fabricated with NaCl containing $In_2O_3$ ink and subsequently heated at 100 °C are shown in Supporting Information Figure S7. Important figures of merit of $In_2O_3$ FETs fabricated without NaCl, with NaCl and dried at 100 °C are listed in Table S1.

**Fabrication of Complementary Metal Oxide Semiconductor (CMOS) Inverters.** CMOS technology has always been essential for logic electronics in order to ensure negligible static power dissipation. Although it may be possible to realize unipolar logics (for example, only with NMOS devices),[35,36] their low signal gain, large power dissipation and poor noise margin values are often not acceptable. In this regard, toward all-oxide CMOS electronics, the problem lies in the fact that an equally good *p*-type oxide semiconductor is rare. Consequently, while there exists at least a few reports on solution-processed hybrid CMOS inverters with *p*-type organic and *n*-type inorganic FETs,[37,38] demonstration of solution-processed and high-performance all-oxide integrated CMOS technology has not yet been reported.

However, here we report not only all-oxide semiconductor channel CMOS logics but also that with a complete room temperature processing. The design strategies (using a high $(W/L)_p$:$(W/L)_n$ ratio) help us to realize high performance logic operation. The CMOS inverters in this case are built using $In_2O_3$ and $Cu_2O$ nanoparticles for the *n*-channel (NMOS) and the *p*-channel (PMOS) MOSFETs, respectively, following the identical PAANa stabilized nanoink preparation and destabilization approach described above. High purity, single phase $Cu_2O$ nanoparticles were synthesized (see Methods for details) and the nanoink was prepared again with the PAANa stabilizer, and 20 mM NaCl as the flocculation agent. Characterization of the $Cu_2O$ nanoparticles and the printed $Cu_2O$ layer with NaCl additive are presented in the

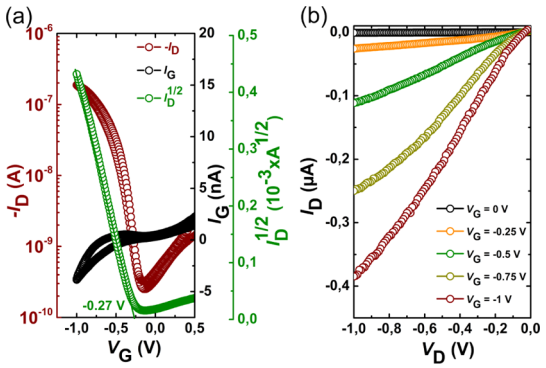


**Figure 4. (a) Transfer and (b) drain current ($I_D$)−drain voltage ($V_D$) curves of a $Cu_2O$ channel PMOS transistor device printed and processed at room temperature. The $Cu_2O$ nanoparticulate channel layer has been fabricated from 20 mM NaCl containing, PAANa stabilized $Cu_2O$ nanoink.**

Supporting Information Figure S8, S9. While the printed $In_2O_3$ nanoparticle films are surprisingly dense and homogeneous, nearly resembling sputtered thin films, the printed $Cu_2O$ films are in comparison found to be relatively granular, which is mainly because of the strongly agglomerated as-synthesized nanopowders, which are not fully fragmented/ruptured during the ink preparation. The effect of this poorer film quality is directly reflected in the electrical performance. The transfer and current−voltage curves of a typical PMOS are shown in Figure 4a,b. The saturated ON current ($I_{D,sat}$), ON/OFF ratio and other transistor characteristics are naturally found mediocre compared to the NMOS devices.

All the passive components of the PMOS devices and the CMOS inverters are again designed by e-beam lithography and structured with sputtered, high work function metal electrodes such as platinum [Cr(2 nm)/Pt(25 nm)], to especially suit the *p*-type semiconductor/metal contact. The channel length of the PMOS and the NMOS are kept 2 and 10 $\mu$m, respectively; the width of the devices has also been varied to end up with a *W*/*L* ratio of PMOS to NMOS equal to 10 [*i.e.*, $(W/L)_p$:$(W/L)_n$ = 10:1]. The voltage transfer, the signal gain and the inverter drive current plots are shown in Figure 5. The voltage gain of the inverter is examined for $V_{DD}$ starting from 0.5 to 1.5 V with an interval of 0.25 V, while keeping GND at 0 V (Figure 5a, inset). The inverter exhibits an ideal rail-to-rail output voltage behavior with a calculated voltage gain ($A_v$ = ($dV_{OUT}$)/($dV_{IN}$)) of around 18 for a supply voltage ($V_{DD}$) of 1.5 V (Figure 5b). A complete switch between 0 and 1.5 V is observed for a $V_{IN}$ of 1.5 and 0 V, respectively. This result is not only the first demonstration of a solution processed all-oxide inverter, or a first room temperature processed oxide electronics, to the best of our knowledge the measured signal gain obtained in this study is also the highest reported value for any oxide electronics to date, even when compared to UHV grown all-sputtered thin film transistors

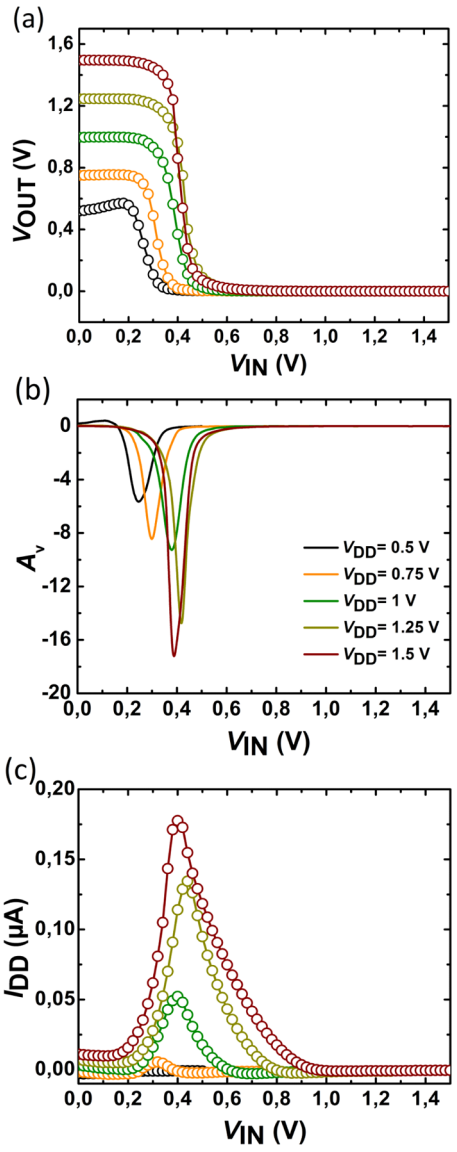


**Figure 5. Electrical characteristics of a typical completely room temperature processed, printed all-oxide CMOS inverter. (a) Output voltage ($V_{OUT}$), (b) Voltage gain ($A_v$) and (c) drive current ($I_{DD}$) of the integrated inverter at different supply voltages ($V_{DD}$) are plotted. The CMOS inverter is comprised of $In_2O_3$ (*n*-type) and $Cu_2O$ (*p*-type) MOSFETs. Inset: the circuit diagram of the CMOS inverter.**

(TFTs).[39] Notably, the measured switching threshold voltage (*i.e.*, when $V_{IN}$ = $V_{OUT}$) is quite close to the ideal value ($V_{DD}$/2)[40] for low $V_{DD}$ (Supporting Information, Table S2); however, it becomes significantly lower with increasing $V_{DD}$ and for $V_{DD}$= 1.5 V it is only 0.39 V; this result suggests unmatched electron and hole mobility and comparatively weaker performance of the *p*-channel MOSFET. However, this in turn leaves a large scope for improvement of the CMOS performance with superior quality of as-prepared $Cu_2O$ nanoparticles. The observed static current is less than 0.5 nA when $V_{DD}$ and $V_{IN}$ is equal to1.5 V (Figure 5c); thus, the static power dissipation is less than 1 nW; such low static power consumption is one of the acclaimed

qualities of CMOS technology. The other important parameter, the noise margin of the logic gate is directly related to the reliability and robustness of the logic circuit: the higher the noise margin is, the more reliable the circuit will be. To ensure a stable operation of an inverter, its high (for logic state "1") and low (for logic state "0") noise margins, $N_{MH}$ and $N_{ML}$ need to be sufficiently positive,[41] ideally both should be close to $V_{DD}/2$. On the other hand, the undefined region (where the output signal is neither "1" nor "0") should be as low as possible. A comparison of noise margins and undefined regions of the inverter for each supply voltage is summarized in Table S2 and a representative plot of the noise margin for a supply voltage of 1.5 V is shown in Supporting Information Figure S10. Again the noise margin values are nearly ideal for low supply voltages, while the undefined region remains fairly constant around 0.2 V for all $V_{DD}$ values.

## CONCLUSION

Complete room temperature processing of *n*- and *p*-type MOSFETs, and CMOS inverters has been demonstrated. The chemically controlled destabilization and flocculation of the nanoparticles during the ink drying step ensure a nearly complete removal of the organic stabilizer from the nanoparticle surface and then an effective reagglomeration of the printed particles (by the strong capillary force). The reduction of the surface energy, the usual driving force toward agglomeration may also contribute in the compaction process. Consequently, high quality, dense and low roughness oxide nanoparticulate films can be printed by one step inkjet printing at room temperature. Furthermore, the chemical flocculation process not only allows for highly dense thin film formation, but it fortunately also removes the polymer stabilizer and thereby reduces the amount of carbon at the nanoparticle surface which is crucial for the formation of high quality semiconductor/dielectric interface. This achievement surmounts a long-standing, formidable challenge to obtain solution-processed high-performance oxide FETs completely at room temperature and without an additional curing step. The $Cu_2O$ and $In_2O_3$ based CMOS logics demonstrated here can be considered as the building blocks for future studies toward large-scale integrated circuits. Moreover, this concept may generally be quite attractive to any other nanomaterials-based devices; high quality, densely packed nanoparticulate films can be prepared just by one step inkjet printing at room temperature and without compromising on their electronic transport properties. Therefore, at a little more speculative level, one can also foresee the use of this technique with other functional nanoparticles, either oxides or nonoxides (*e.g.*, sulfides or selenides), for printed electronic devices beyond printed logics, for example, sensors, photovoltaics, *etc*.

## METHODS

**Nanoparticle Preparation.** Copper oxide ($Cu_2O$) nanoparticles were synthesized as follows.[42] 12 g of $Cu(NO_3)_2 \cdot 2.5H_2O$ and 14 mL of triethanolamine (TEA) was dissolved in 400 mL of DI water. In order to ensure a homogeneous solution, it was then stirred for about 30 min. Next, under continuous stirring 17 mL of 6 M NaOH was added dropwise to the solution to precipitate $Cu(OH)_2$, followed by an addition of nearly 2 mL of 13.7 M $N_2H_4 \cdot H_2O$, which then completely reduced the precipitated to $Cu_2O$, thus the color of the precipitate gradually turned red. At the end, the precipitate was carefully collected by filtration and washed several times with ample amount of distilled water, and finally dried in a vacuum oven at 60 °C for overnight.

**Nanoink Preparation.** The printable grade of semiconducting nanoparticulate ink was prepared from commercially available indium oxide ($In_2O_3$) nanoparticles (Plasmachem GmbH) and self-made $Cu_2O$ nanoparticles. Double-distilled water was used as the ink solvent; the nanoparticle loading was limited to 10 wt % to obtain a long-term stable nanodispersion. Sodium salt of poly acrylic acid (PAANa) (Sigma-Aldrich) was used as the stabilizer. The optimum loading of the stabilizer was found to be around 10 wt % of the weight of the oxide nanoparticles. A homemade dispersing unit based on a commercially available dissolver/mixer (Dispermat) was used to prepare the nanodispersion/nanoink. The ink preparation process was analogous to a liquid media milling process, where 0.2−0.3 mm diameter zirconia pearls were used as the milling material in order to break the large agglomerates. The nanoparticles−stabilizer mixture was spun with the zirconia pearls for 90 min at a rotational speed of 8000 rpm, which was then followed by a separation process for zirconia pearls and the remaining large agglomerates, by a series of filtration steps through 5, 0.45, and 0.2 $\mu$m syringe filters, respectively.

**Composite Solid Polymer Electrolyte Preparation.** The composite solid polymer electrolyte was prepared in a similar manner as had already been reported in our earlier publications.[22,29] The electrolyte consists of four essential ingredients: the synthetic polymer, poly(vinyl alcohol) (PVA, average $M_w$ = 13−23 kDa, 98% hydrolyzed, Sigma-Aldrich); the plasticizer, propylene carbonate (PC, anhydrous, 99.7%, Sigma-Aldrich); the solvent, dimethyl sulfoxide (DMSO, anhydrous 99.9%, Sigma-Aldrich) and the supporting electrolyte/salt lithium perchlorate ($LiClO_4$, anhydrous, 98%, Alfa Aesar); all these components were used as-received without any further purification. First, the necessary amount of PVA (0.3 g) was dissolved in DMSO (6 g) by heating at 90 °C and continuously stirring for about an hour; simultaneously, in a different container $LiClO_4$ (0.07 g) crystals were dissolved in PC (0.63 g). In the next step, both solutions were mixed together at room temperature and stirred for another 12−24 h in order to obtain a completely homogeneous solution. The resultant solution was then filtered through a 0.2 $\mu$m syringe filter. The respective concentration of the constituents was optimized for the finest performance of the polymer-gel electrolyte; the PVA:PC:$LiClO_4$ ratio was kept at 30:63:7; to ensure that the viscosity of the polymer electrolyte falls within the preferred window of inkjet printing, the weight of DMSO was taken 6 times larger compared to the total weight of all the other components together.

**Device Fabrication.** $In_2O_3$ FETs were built using tin doped indium oxide (ITO) passive structures. The source (S), the drain (D) and the gate (G) electrodes were defined by e-beam lithography and fabricated with 150 nm sputtered ITO. The channel length in this case was kept constant at 10 $\mu$m. The PAANa stabilized $In_2O_3$ nanoinks with or without NaCl were printed on these prestructured electrodes. In contrast to the NMOS devices, in case of CMOS inverters, sputtered metallic [Cr(2 nm)/Pt(25 nm)] thin films were used to fabricate the

passive structures for both $In_2O_3$ nanoparticle-based NMOS and $Cu_2O$ nanoparticle-based PMOS devices. $Cu_2O$ and $In_2O_3$ nanoinks were printed separately at the respective locations using two individual cartridges. After complete drying of the semiconductor nanoinks forming the FET channel, the nonaqueous polymer electrolyte was printed in a way to completely cover the channel area, and partially the gate electrode. All the printing steps were carried out with commercially available Dimatix DMP 2831 inkjet printer.

**Characterization of Oxide Nanoparticles, Nanoink and Surface/Cross-Sectional Morphology of the Printed Nanoparticle Layers.** X-ray diffraction measurements on the as-received $In_2O_3$ nanoparticles were performed using a PANalytical X'PERT Pro X-ray diffractometer with nickel-filtered Cu Kα radiation as the X-ray source. The surface morphology of the printed nanoparticulate layer and the cross-section of the printed devices with electrolytic gate insulator were investigated with a Leo 1530 scanning electron microscope (SEM). The height of the printed layer was examined by profiling with a Dektak 6 M stylus profiler with the N-Lite low force package (Veeco). Electrical measurements were performed using Agilent 4156C semiconductor parameter analyzer and Süss MicroTec, EP6 probe station. All the electrical measurements were carried out at ambient conditions and at room temperature.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Characterization of oxide nanoparticles, surface profile of printed $In_2O_3$ droplets, calculation of electrical double layer capacitance, $Cu_2O$ nanoink characterizations and CMOS inverter characteristics are included. This material is available free of charge *via* the Internet at http://pubs.acs.org.

## REFERENCES AND NOTES


1. Sun, K.; Wei, T. S.; Ahn, B. Y.; Seo, J. Y.; Dillon, S. J.; Lewis, J. A. 3D Printing of Interdigitated Li-ion Microbattery Architectures. *Adv. Mater.* **2013**, *25*, 4539–4543.
2. Street, R. A.; Wong, W. S.; Ready, S. E.; Chabinyc, M. L.; Arias, A. C.; Limb, S.; Salleo, A.; Lujan, R. Jet Printing Flexible Displays. *Mater. Today* **2006**, *9*, 32–37.
3. Abargues, R.; Rodriguez-Canto, P. J.; Albert, S.; Suarez, I.; Martínez-Pastor, J. P. Plasmonic Optical Sensors Printed from Ag−PVA Nanoinks. *J. Mater. Chem. C* **2014**, *2*, 908–915.
4. Martínez-Olmos, A.; Fernández-Salmerón, J.; Lopez-Ruiz, N.; Torres, A. R.; Capitan-Vallvey, L. F.; Palma, A. J. Screen Printed Flexible Radiofrequency Identification Tag for Oxygen Monitoring. *Anal. Chem.* **2013**, *85*, 11098–11105.
5. Hamedi, M.; Herlogsson, L.; Crispin, X.; Marcilla, R.; Berggren, M.; Inganäs, O. Fiber-Embedded Electrolyte-Gated Field-Effect Transistors for e-Textiles. *Adv. Mater.* **2009**, *21*, 573–577.
6. Xu, L.; Gutbrod, S. R.; Bonifas, A. P.; Su, Y.; Sulkin, M. S.; Lu, N.; Chung, H. J.; Jang, K. I.; Liu, Z.; Ying, M.; *et al.* 3D Multifunctional Integumentary Membranes for Spatiotemporal Cardiac Measurements and Stimulation Across the Entire Epicardium. *Nat. Commun.* **2014**, *5*, 3329–10.
7. Rogers, J. A. Toward Paperlike Displays. *Science* **2001**, *291*, 1502–1503.
8. Sun, Y.; Rogers, J. A. Inorganic Semiconductors for Flexible Electronics. *Adv. Mater.* **2007**, *19*, 1897–1916.
9. Fortunato, E.; Barquinha, P.; Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **2012**, *24*, 2945–2986.
10. Dasgupta, S.; Kruk, R.; Mechau, N.; Hahn, H. Inkjet Printed, High Mobility Inorganic-Oxide Field Effect Transistors Processed at Room Temperature. *ACS Nano* **2011**, *5*, 9628–9638.
11. Garlapati, S. K.; Mishra, N.; Dehm, S.; Hahn, R.; Kruk, R.; Hahn, H.; Dasgupta, S. Electrolyte-Gated, High Mobility Inorganic Oxide Transistors from Printed Metal Halides. *ACS Appl. Mater. Interfaces* **2013**, *5*, 11498–11502.
12. Chiang, H. Q.; Wager, J. F.; Hoffman, R. L.; Jeong, J.; Keszler, D. A. High Mobility Transparent Thin-Film Transistors with Amorphous Zinc Tin Oxide Channel Layer. *Appl. Phys. Lett.* **2005**, *86*, 013503-3.
13. Schneider, J. J.; Hoffmann, R. C.; Engstler, J.; Soffke, O.; Jaegermann, W.; Issanin, A.; Klyszcz, A. A. A Printed and Flexible Field-Effect Transistor Device with Nanoscale Zinc Oxide as Active Semiconductor Material. *Adv. Mater.* **2008**, *20*, 3383–3387.
14. Hirschmann, J.; Faber, H.; Halik, M. Concept of a Thin Film Memory Transistor Based on Zno Nanoparticles Insulated by a Ligand Shell. *Nanoscale* **2012**, *4*, 444–447.
15. Kim, M. G.; Kanatzidis, M. G.; Facchetti, A.; Marks, T. J. Low-Temperature Fabrication of High-Performance Metal Oxide Thin-Film Electronics *via* Combustion Processing. *Nat. Mater.* **2011**, *10*, 382–388.
16. Banger, K. K.; Yamashita, Y.; Mori, K.; Peterson, R. L.; Leedham, T.; Rickard, J.; Sirringhaus, H. Low-Temperature, High-Performance Solution-Processed Metal Oxide Thin-Film Transistors Formed by a 'Sol−Gel On Chip' Process. *Nat. Mater.* **2011**, *10*, 45–50.
17. Perelaer, J.; Jani, R.; Grouchko, M.; Kamyshny, A.; Magdassi, S.; Schubert, U. S. Plasma and Microwave Flash Sintering of a Tailored Silver Nanoparticle Ink, Yielding 60% Bulk Conductivity on Cost-Effective Polymer Foils. *Adv. Mater.* **2012**, *24*, 3993–3998.
18. Kim, Y. H.; Heo, J. S.; Kim, T. H.; Park, S.; Yoon, M. H.; Kim, J.; Oh, M. S.; Yi, G. R.; Noh, Y. Y.; Park, S. K. Flexible Metal-Oxide Devices Made by Room-Temperature Photochemical Activation of Sol−Gel Films. *Nature* **2012**, *489*, 128–132.
19. Golas, P. L.; Louie, S.; Lowry, G. V.; Matyjaszewski, K.; Tilton, R. D. Comparative Study of Polymeric Stabilizers for Magnetite Nanoparticles Using ATRP. *Langmuir* **2010**, *26*, 16890–16900.
20. Grouchko, M.; Kamyshny, A.; Mihailescu, C. F.; Anghel, D. F.; Magdassi, S. Conductive Inks with a "Built-In" Mechanism That Enables Sintering at Room Temperature. *ACS Nano* **2011**, *5*, 3354–3359.
21. Magdassi, S.; Grouchko, M.; Berezin, O.; Kamyshny, A. Triggering the Sintering of Silver Nanoparticles at Room-Temperature. *ACS Nano* **2010**, *4*, 1943–1948.
22. Dasgupta, S.; Stoesser, G.; Schweikert, N.; Hahn, R.; Dehm, S.; Kruk, R.; Hahn, H. Printed and Electrochemically Gated, High-Mobility, Inorganic Oxide Nanoparticle FETs and Their Suitability for High-Frequency Applications. *Adv. Funct. Mater.* **2012**, *22*, 4909–4919.
23. Stamenković, J. V.; Premović, P. I.; Mentus, S. V. Electrical Conductivity of Poly(Acrylic Acid) Gels. *J. Serb. Chem. Soc.* **1997**, *62*, 945–950.
24. Siddons, G. P.; Merchin, D.; Back, J. H.; Jeong, J. K.; Shim, M. Highly Efficient Gating and Doping of Carbon Nanotubes with Polymer Electrolytes. *Nano Lett.* **2004**, *4*, 927–931.
25. Panzer, M. J.; Frisbie, C. D. Polymer Electrolyte-Gated Organic Field-Effect Transistors: Low-Voltage, High-Current Switches for Organic Electronics and Testbeds for Probing Electrical Transport at High Charge Carrier Density. *J. Am. Chem. Soc.* **2007**, *129*, 6599–6607.
26. Herlogsson, L.; Crispin, X.; Tierney, S.; Berggren, M. Polyelectrolyte-Gated Organic Complementary Circuits Operating at Low Power and Voltage. *Adv. Mater.* **2011**, *23*, 4684–4689.
27. Lee, J.; Panzer, M. J.; He, Y.; Lodge, T. P.; Frisbie, C. D. Ion Gel Gated Polymer Thin-Film Transistors. *J. Am. Chem. Soc.* **2007**, *129*, 4532–4533.
28. Hong, K.; Kim, S. H.; Lee, K. H.; Frisbie, C. D. Printed, Sub-2V Zno Electrolyte Gated Transistors and Inverters on Plastic. *Adv. Mater.* **2013**, *25*, 3413–3418.
29. Nasr, B.; Wang, D.; Kruk, R.; Rösner, H.; Hahn, H.; Dasgupta, S. High-Speed, Low-Voltage, and Environmentally Stable Operation of Electrochemically Gated Zinc Oxide Nanowire Field-Effect Transistors. *Adv. Funct. Mater.* **2013**, *23*, 1750–1758.

30. Salahuddin, S.; Datta, S. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. *Nano Lett.* **2008**, *8*, 405–410.
31. Sze, S. M. *Physics of Semiconductor Devices*, 2nd ed.; John Wiley & Sons: New York, 1981; pp 438−442.
32. Panzer, M. J.; Frisbie, C. D. Polymer Electrolyte Gate Dielectric Reveals Finite Windows of High Conductivity in Organic Thin Film Transistors at High Charge Carrier Densities. *J. Am. Chem. Soc.* **2005**, *127*, 6960–6961.
33. Ha, M.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks. *ACS Nano* **2010**, *4*, 4388–4395.
34. Ha, M.; Seo, J. T.; Prabhumirashi, P. L.; Zhang, W.; Geier, M. L.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Aerosol Jet Printed, Low Voltage, Electrolyte Gated Carbon Nanotube Ring Oscillators with Sub-5 $\mu$s Stage Delays. *Nano Lett.* **2013**, *13*, 954–960.
35. Hwang, T.-H.; Yang, I.-S.; Kwon, O.-K.; Ryu, M.-K.; Byun, C.-W.; Hwang, C.-S.; Park, S.-H. K. Inverters Using Only N-Type Indium Gallium Zinc Oxide Thin Film Transistors for Flat Panel Display Applications. *Jpn. J. Appl. Phys.* **2011**, *50*, 03CB06-4.
36. Debnath, P. C.; Lee, S. Y. Full Swing Logic Inverter with Amorphous Siinzno and Gainzno Thin Film Transistors. *Appl. Phys. Lett.* **2012**, *101*, 092103-3.
37. Chen, H.; Cao, Y.; Zhang, J.; Zhou, C. Large-Scale Complementary Macroelectronics Using Hybrid Integration of Carbon Nanotubes and IGZO Thin-Film Transistors. *Nat. Commun.* **2014**, *5*, 4097-12.
38. Dhananjay, O. C. -W.; Yang, C.-Y.; Wu, M.-C.; Chu, C.-W. Ambipolar Transport Behavior in $In_2O_3$/Pentacene Hybrid Heterostructure and Their Complementary Circuits. *Appl. Phys. Lett.* **2008**, *93*, 033306-3.
39. Martins, R. F. P.; Ahnood, A.; Correia, N.; Pereira, L. M. N. P.; Barros, R.; Barquinha, P. M. C. B.; Costa, R.; Ferreira, I. M. M.; Nathan, A.; Fortunato, E. E. M. C. Recyclable, Flexible, Low-Power Oxide Electronics. *Adv. Funct. Mater.* **2013**, *23*, 2153–2161.
40. Wang, C.; Ryu, K.; Badmaev, A.; Zhang, J.; Zhou, C. Metal Contact Engineering and Registration-Free Fabrication of Complementary Metal-Oxide Semiconductor Integrated Circuits Using Aligned Carbon Nanotubes. *ACS Nano* **2011**, *5*, 1147–1153.
41. Tosun, M.; Chuang, S.; Fang, H.; Sachid, A. B.; Hettick, M.; Lin, Y.; Zeng, Y.; Javey, A. High-Gain Inverters Based on $WSe_2$ Complementary Field-Effect Transistors. *ACS Nano* **2014**, *8*, 4948–4953.
42. Wang, W. Z.; Wang, G. H.; Wang, X. S.; Zhan, Y. J.; Liu, Y. K.; Zheng, C. L. Synthesis and Characterization of $Cu_2O$ Nanowires by a Novel Reduction Route. *Adv. Mater.* **2002**, *14*, 67–69.